# Dynamically Reconfigurable Imager for Real-Time Staring Vision Systems

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**ABSTRACT**

*Design and characterization of a high-performance multi-acuity, multi-window dynamically reconfigurable vision (DRV) CMOS imager for real-time staring vision systems is presented. By carrying out on-focal-plane image preprocessing, the imager chip simultaneously supports low-resolution large field-of-view (FOV) scan and high-resolution narrow FOV tracking. As a result, data bottleneck inherent in full-frame operating mode is greatly eliminated, allowing high update rates (> 1 kHz), and simultaneous data capture from three partially overlapping reconfigurable regions of interest (ROIs). As a result, the imager enables a low-power staring vision system that concurrently meets the diverse and conflicting requirements of search, identify and track modes of imaging.*

## I. INTRODUCTION

Active vision systems are of great interest in realizing autonomous systems ranging from commercial to surveillance, military, and future space applications. The complexity of an active vision system arises from the fact that it concurrently carries out a number of diverse visual tasks, such as search, detection, recognition, and multi-target tracking. Search requires wide field-of-view (FOV), tracking requires fast frame rate data output from regions of interest (ROI), recognition requires high spatial resolution, while multi-target cueing requires all three of them concurrently. These cannot be easily handled by imaging systems with conventional image sensors due to the serial nature of pixel access and the enormity of the data volume. For example, a large FOV system consisting of a million pixels, operating with an update rate of 1 kHz digitized to 10 bits will require a data output rate at a prohibitively high data rate of 10 Gigabits per second, not to mention the enormity of data storage needed.

Moreover, data processing complexity grows as a function of $n^M$, where n is the number of pixels output to the off-chip processor, and M > 1. Thus, the elimination of data-redundancy is critical for realization of real-time, miniature active vision systems with low-power dissipation. Biological systems achieve real-time imaging through the use of foveated architectures. Foveal vision allows acquisition of image with varying spatial resolution that is coarser at the periphery and more refined at the center (the fovea). Although imagers with the pixel sizes scaled and organized in a foveal topology have been demonstrated [1], such devices provide only serial access, and consist of hard-wired (i.e. non-programmable) acuity variation. Consequently, such vision system requires mechanical pointing. The size, power consumption, stability, and the slow response times of mechanical pointing systems preclude an efficient realization of a low-power, miniature, real-time active vision system.

In this work, we present the design and characterization results of a high-performance multi-acuity, multi-window dynamically reconfigurable vision (DRV) CMOS imager. The imager is capable of simultaneously providing data from three partially overlapping ROIs, with the locations and resolutions of the ROIs being dynamically reconfigurable by the user. The imager is capable of operation in tracking mode at > 1kHz update rates. By allowing placement of the high resolution "fovea" anywhere within the FOV, the imager enables a low-power staring active vision system that meets the diverse and conflicting requirement of search, identify and track modes.

## II. RECONFIGURABLE VISION SYSTEM

The DRV system consists of a CMOS imager capable of supporting multi-resolution, multi-ROI imaging at high speed, and a processor for providing user inputs and data acquisition. Unlike a traditional foveal vision, the reconfigurable foveal vision system adapts its acuity profile on a frame-by-frame basis to improve update rates, and to eliminate altogether mechanical gazing. Targets are initially detected in the system's default wide FOV, fast frame rate, and coarse acuity configuration. The reconfiguration of the topology of the foveal vision system is illustrated in figure 1. Targets are initially detected in a wide FOV, fast frame rate, and coarse acuity configuration. Following detection, spatial resolution is increased only in the vicinity of the detected objects in order to better resolve targets without wasting system resources on irrelevant scene regions. The coarse-to-fine refinement is analogous to pyramid machine vision techniques [2], except that the DRV system does not require generation of the complete pyramid data structure or the overhead due to high-resolution, wide-FOV, uniform acuity imagery [3].

## III. IMAGER DESIGN AND OPERATION

The imager in the DRV system is a 256x256 photogate snapshot [4] imager chip, implemented in a 0.5-µm n-well 1P3M process. The schematic block diagram of the imager is shown in figure 2. It consists of a CMOS pixel array, integrated column-parallel signal processing circuits at the top and bottom of the imagers, column and row control circuits, and interface control logic. Two of the ROIs (window 2 & 3) are controlled by the control blocks located at the bottom of the imager and are output from port #2, while window-1 control and output is located at the top of the imager array. The architecture does not require any modification of the pixel array, since variable ROI resolution is accomplished through column-parallel circuits. This permits multi-resolution output without sacrificing imaging performance. Variable resolution ROI or a superpixel is implemented by averaging a block of mxn neighboring of pixels, using a column-parallel switched capacitor array to carry out passive averaging [5].

The imager is designed to support only a set of binary selectable ROI resolutions, with the resolutions scaled in a binary fashion from 1x1 to 32x32. Thus, there are six different super-pixel resolution settings, although multiple adjoining super-pixels can be grouped together to create arbitrarily large ROIs. The ROI-1 (window-1) can overlap with ROI-2 and ROI-3.

Unlike a conventional imager, the DRV imager requires special column control logic signals in order to configure the ROIs and generate super-pixel data. Six control bits per column are needed for each ROI to control the row-averaging, column-averaging and readout functions. Since the ROIs can have arbitrary starting positions and sizes, as well as different resolutions (i.e. super-pixel depths), the control bit pattern for each ROI is different. Individual ROI bit-patterns are separately generated, followed by multiplexing and latching on column-latches for simultaneous control of the ROIs.

Unlike a shift-register-based column logic reported earlier [5], the DRV chip uses static column-control logic in order to provide high speed readout. A diagonal switch array is used to upload the block-averaging switch-patterns at the appropriate ROI column start locations. In addition, an EXOR based logic is used to generate a select "mask" to ensure that only columns belonging to the ROIs are selected. Although the mask is generated in a ripple fashion, the setup time is small, since gate delays for sub-micron CMOS technologies are of the order of 5 psec. The maximum setup time for a 1024x1024 imager is less than 100 nsec, allowing imager operation with minimal overhead time.

On-chip power dissipation is minimized by sampling only those columns that contain active ROI data. For this purpose, an additional control line is used to disable the unnecessary column source-followers during row sampling. In order to accommodate all seven column-control lines, minimum pixel pitch is restricted to about 12 µm for advanced 0.5 µm CMOS process. The prototype chip is designed with 15 µm pixel pitch.

## IV. IMAGER PERFORMANCE

More than 100Hz frame rate has been achieved at all window sizes and super-pixel resolutions. A very high update rate of 10 kHz was reached for an ROI consisting of 10x10 super-pixels, with each super-pixel consisting of block-averaged 4x4 pixels. Averaging error was found to be less than 0.7%, and to depend only slightly on the super-pixel size.

The use of photogate pixels allows imaging with ultra-low noise, and moderate quantum efficiency. Less than 7 electrons were measured at 2 MHz data output rates. Imager power dissipation is low and is dependent on the super-pixel size. For full-frame readout, power dissipation increases from 5 to 15 mW at 2 Mpix/sec. for super-pixel size ranging from 1x1 to 32x32. Figure 3 shows the image captured in snap-shot mode.

A prototype DRV unit was built around the DRV imager. It consists of the DRV camera, a host laptop, and an ethernet data link. The host displays video from 3 concurrent DRV windows over a fast Ethernet (100 Mbps) data link. Overall timing and control signals are provided by an embedded programmable logic device (PLD). Figure 4 shows the picture of the camera unit, and figure 5 demonstrates the operation of the unit with simultaneous display of wide-FOV lower-resolution and narrow-FOV high-resolution imagery. A template-based external tracking scheme was used to continuously track the two persons in the FOV at 25 FPS [6]. Table 1 summarizes the performance characteristics and important experimental results of the DRV imager.

## VI. CONCLUSIONS

In summary, we have presented the design and operation of a large-format reconfigurable multi-ROI, multi-resolution CMOS imager. The imager is capable of simultaneously imaging from 3 separate ROIs with different resolutions that are user-selectable. Update rates in excess of 10 kHz can be reached with less than 7 electrons read noise. The total power dissipation, including the control and signal processing circuits is between 15 mW. The imager is versatile enough to handle imaging efficiently and concurrently with wide-FOV and high resolution.

## ACKNOWLEDGMENT

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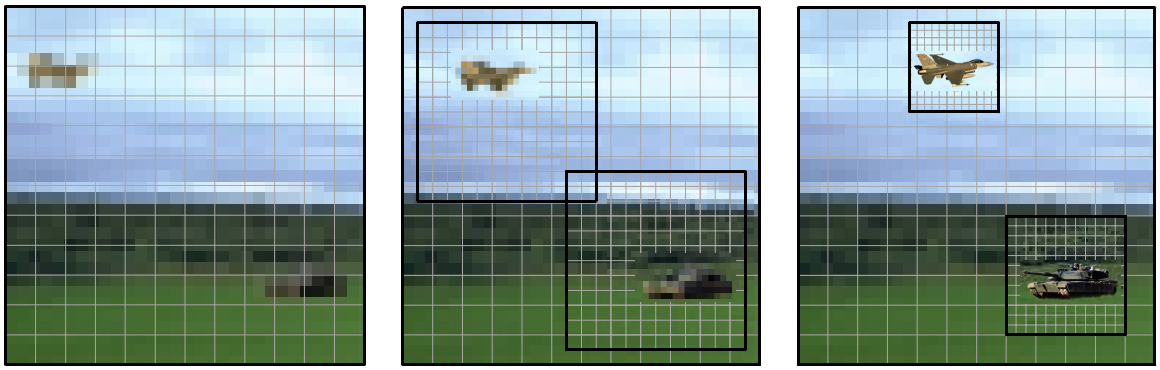

**Figure 1.** Conceptual target acquisition and tracking using DRV imaging system.

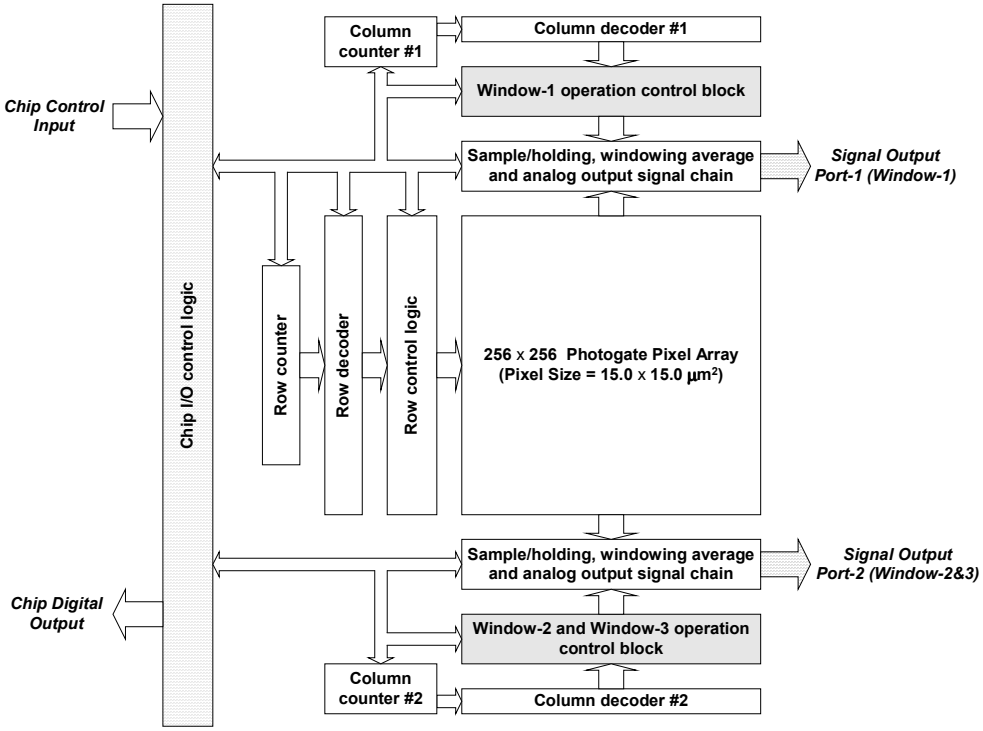


**Figure 2.** Schematic showing the block diagram of the DRV imager.

**Table 1**. DRV imager performance characteristics and important experimental results.

| Characteristics | Values | Comments |
|---|---|---|
| *Imager format* | 256x256 | |
| *Pixel Type* | Photogate | *Snapshot operation* |
| *Pixel Pitch* | 15-µm x 15-µm | |
| *Number of simultaneous ROIs* | 3 | |
| *Max. Update rate* | 100 kHz | |
| *Super-pixel sizes* | 1x1, 2x2, 4x4, 8x8, 16x16, 32x32 | *6 super-pixel resolutions* |
| *Averaging Error* | < 0.7% | |
| *Quantum Efficiency* | 22 % | *@ 550 nm* |
| *Full-well* | 45000 $e^-$ | |
| *Noise* | < 7 electrons | *@ 2MHz data output rate* |
| *Dynamic range* | > 75 dB | *For short-exposure time* |
| *Imager FPN* | ~ 0.1% of imager saturation level | *Not visible* |
| *Dark current* | 100 pA/cm$^2$ | *@ Room temperature* |

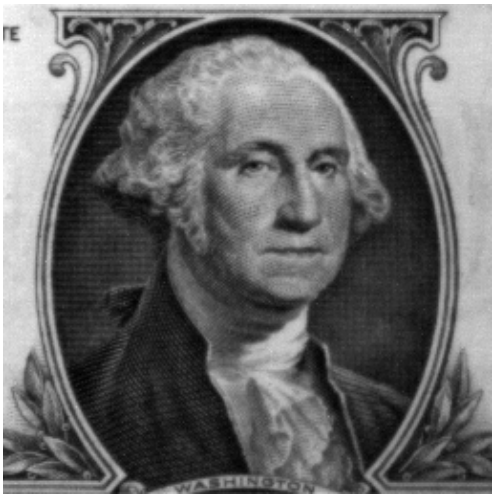

**Figure 3.** 256x256 Image captured in snap-shot mode of operation.

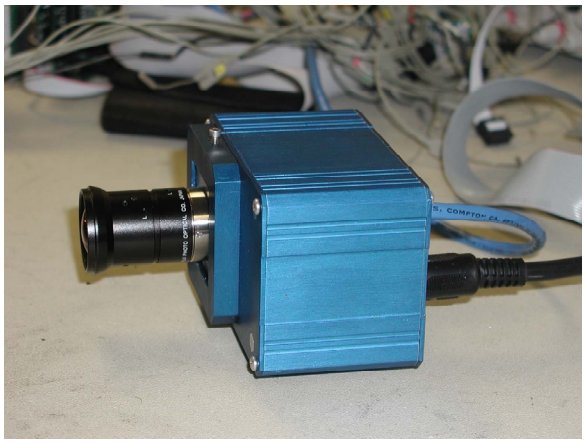

**Figure 4.** Picture of the DRV demonstration unit.

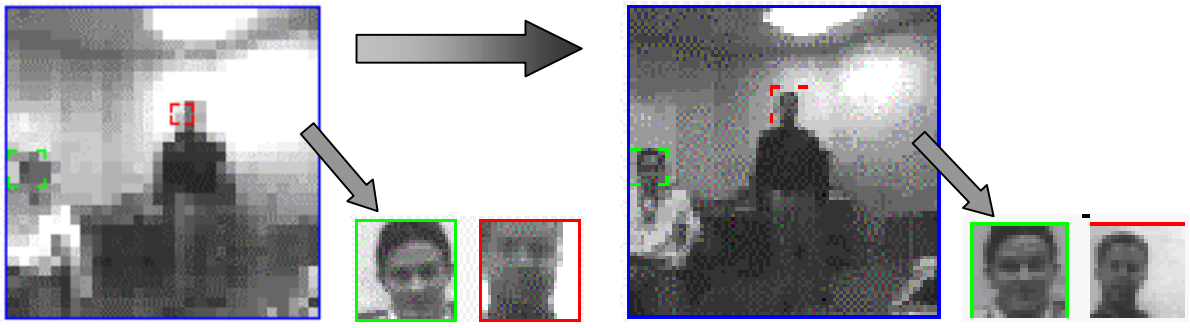

**Figure 5.** Two frames of DRV image data from windows. One window operates at low-resolution wide FOV, and the other two embedded within the FOV operates at higher resolution narrow FOV.