A High Speed, 240 Frame/s, 4 Megapixel CMOS Sensor

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Abstract

The paper describes a large format 4 Megapixel (2352x1728) sensor with on-chip parallel 10 bit ADCs. The chip size is 20 x 20 mm with 7 μm pixel pitch. It achieves a high frame rate of 240 frames/s delivering 9.75 Gbit of data per second. The sensor also features an additional fixed pattern noise cancellation circuitry. The sensor operation voltage is 3.3 V with power dissipation of ~1 W at master clock rate of 66 MHz. Principal architecture of the sensor is discussed along with the results of its characterization.

Introduction

CMOS sensors are rapidly advancing in high-speed imaging. Compared to high-speed CCDs, with a degree of parallelism represented by the number of panels, CMOS sensors utilize the natural advantage of a column-parallel readout from the pixels. Row processing time can be readily reduced to one microsecond and lower, and the high-speed design focuses on such challenges as the column-multiplexing, ADC, and the reduction of system noise. Another advantage of a CMOS sensor to CCD is practically no smear nor blooming.

Two years ago, a 1Mpixel digital image sensor with rolling shutter running at 500 Frames per second was presented [1]. It was an order improvement in data rate compared to the state-of the art high-speed CMOS sensors. Since that time, the progress was steady, but gave only about a factor of 2 increase in data throughput over 2 years. Mostly, the efforts were centered on the development of the pixels with full-frame shutter, featuring competitive performance. We believe that the state-of-the-art by the end of 2001 would be a 1K x 1K x 1K sensor (1000 Fps) with a shutter pixel. It is very likely that the progress in high speed CMOS imaging for many years in a row will still be defined by column-parallel architectures. However, a new generation of digital sensors [2] utilizing a higher, pixel-level degree of parallelism and using the benefits of the scaling along with the mainstream digital CMOS technology may be an additional path to high speed image capture.

This article presents a chip, which is a result of the direct evolution of the baseline high-speed digital sensor design [1]. The architecture did not change much, but the following improvements were made:

- resolution was increased 4 times, from 1024x1024 to 2352x1728,
- column-parallel ADC evolved from 8 to 10 bit,
- temporal and fixed-pattern noise was reduced,
- sensitivity was improved.

The overall throughput increased from 4 Gbit/s to almost 10 Gbit/s.

Sensor building blocks

The sensor block diagram is presented in Fig.1. In addition to the pixel array based on the conventional 3T APS pixel, the sensor contains column-parallel ADCs and memory, column and row decoders, row drivers, and two controllers to run concurrently row operations including A/D conversion and read-write memory operations.

Circuit solutions for these blocks did not change much since the previous design, so we refer the reader to [1] for details. One thing that changed about the ADC is that in order to achieve 10 bit operation without using too large capacitors, we generated a reference voltage equal of ¼ of the ADC reference and used larger capacitors for 3 of the less significant bits.

Sensor resolution, 2352x1728 was defined by a customer and, although it did not represent any up-to-date industry standard, it has a very useful aspect ratio of 4:3. Also, the sensor can support a Super XGA (2048x1536) format just emerging on the computer market. And, the chip can be used as a high speed HDTV imager with sub-resolution of 1920x1080 (Fig.2.). The sensor was designed so that the row operations are completed in 128 clocks. This corresponds to reading out of 2048 columns. Thus, the speed in sub-resolution modes can be further increased by skipping the rest of unread columns. Of course, this is in addition to the reduction of the frame time with less number of rows in the frame.

Direct external addressing to the rows gives the user a flexibility of selecting the window of interest within the center of the pixel array, achieving maximum photoresponse uniformity.

The earlier 1Mpixel sensor had an offset-calibration circuit for each ADC. However, the resolution of the internal compensation DAC was only 5 bits. In the reported sensor, the DAC resolution was increased to 7 bits. In addition, a read/write access to the calibration DACs is provided through a serial interface. This yields stability of calibration vectors during the sensor operation. Also, if for some reasons, the internal calibration does not fully remove column-wise fixed pattern noise, the values can be calculated externally and downloaded into the chip.

Layout and CMOS process

The floorplan of the chip layout is outlined in Fig.3. ADCs and memory are split between the top and the bottom for symmetry, performance, and routing considerations. Digital pads are on the left, and at the top/bottom. Analog pads are to the right.

The pixel array area slightly exceeds 1’’ format. The chip with the size of 20mm x 20mm fits into one reticule.

Wafers were fabricated in a 0.35um CMOS sensor process with double poly used for capacitors and triple metal for routing.

Characterization results

The sensor was characterized using a custom board with a frame grabber and a PC interface. The board provided 9 upper bits image recording. So the lsb in the following pictures represents the second bit. By the time of writing the paper, only limited characterization using only green light has been done. All the measurements were performed for the sensor running at 130 frames/s and for 1V ADC reference voltage. The results of the characterization are summarized in Table.1.

Table 1

Technology	0.35um 2P3M
Resolution	2352x1728
Maximum frame rate	240 Frames/s
Pixel	7um, ERS
Responsivity @550nm	2.5 V/Lux-s
QE*FF @550nm	40%
Noise	50e- rms
DSNU, (w/o f.p.n. cancellation)	90e- r.m.s.
Conversion gain	30 uV/e
Dynamic range @1V ADC reference	54 dB
ADC	10 bit
Number of outputs	16 x 10 bit
Power supply	3.3V
Power	1W
Package	280 PGA

The sensor demonstrates good sensitivity and quantum efficiency, higher than in the previous sensor with larger 10um pixel. The fundamental noise is the same. However, the 1Mpixel sensor had an excessive electronic noise at 500 frames/s approaching 120e- if the image went through a massive major bit transition. In the reported sensor, the readout noise was reduced to only 30e- yet contributing little into the overall noise. Dark fixed-pattern noise was relatively small even without the additional f.p.n. correction circuit (90e- r.m.s. over the entire pixel array). The dynamic range was 54 dB at 1V ADC reference, which is less than in the previous sensor. This is because of a smaller photodiode capacitance and hence pixel handling capacity. Although, the dynamic range could be increased by another 5 dB with a higher ADC reference at the cost of lower responsivity.

Fig.4 shows the square of noise as a function of signal. This is a typical measurement of the conversion gain. From this plot, the conversion gain at the ADC output was 0.02 bit/e- (assuming the 9 bit operation). Table 1 reports the performance referred to the pixel floating diffusion.

A sample image taken with the sensor is shown in the last figure.

Conclusions

We presented a high speed 4 Megapixel CMOS sensor and reported the results of its characterization. The sensor targets high speed camera market, scientific, industrial, and military applications, and also can be used for high speed HDTV.

Acknowledgment

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References

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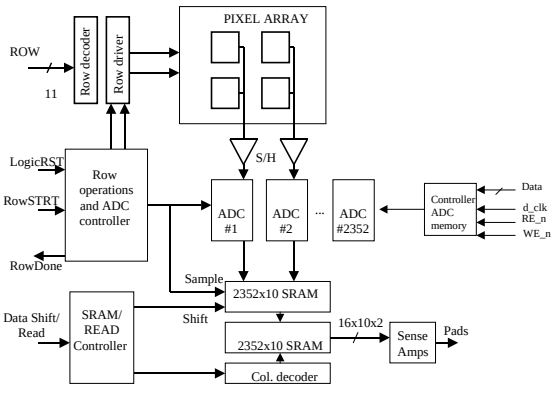

Fig.1. Block diagram of the sensor

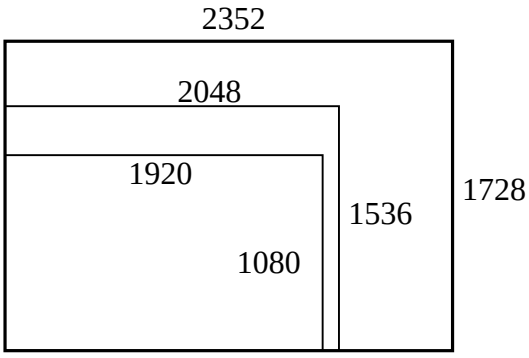

Fig.2. The sensor supports 2368x1536 display mode, and 1920x1080 HDTV format.

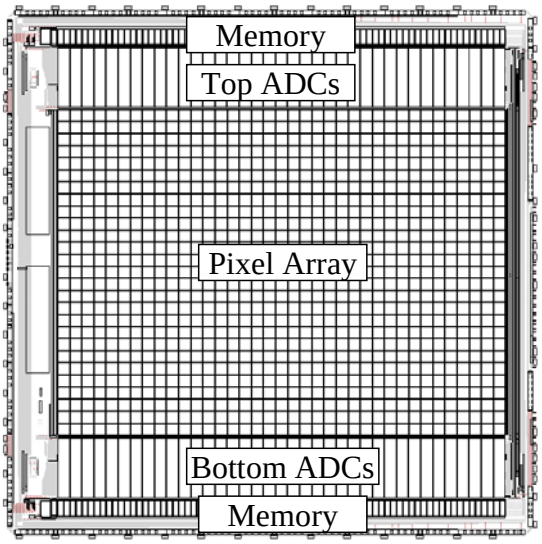

Fig.3. The floorplan of the chip

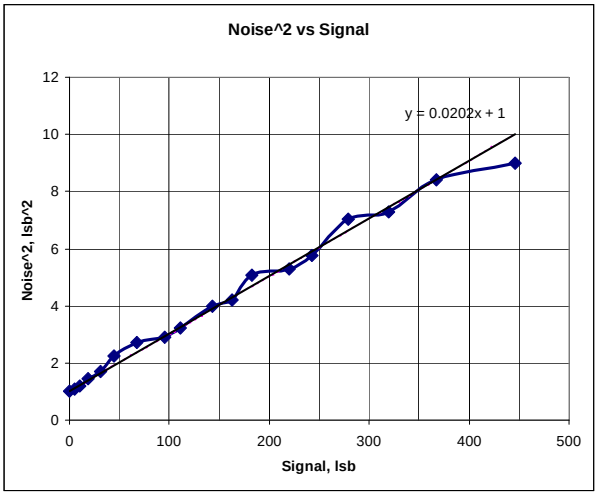

Fig.4. Conversion gain measurements

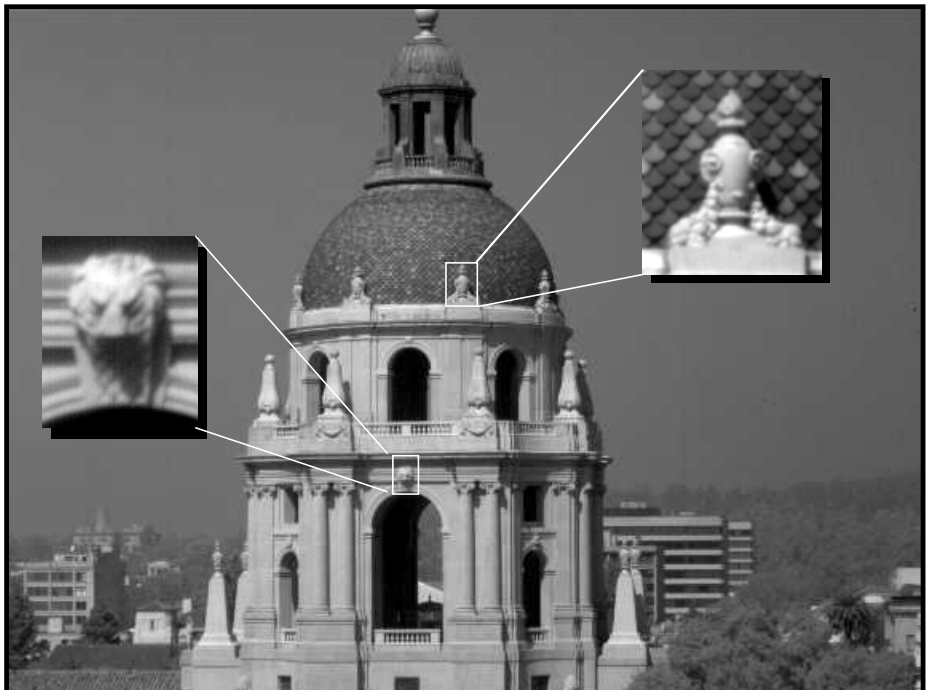

Fig.5. Image of Pasadena City Hall.