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Real-time Calibration of a 14-Bit Single Slope ADC with 290MHz On-chip Accelerated Ramp Generator for Column-Parallel Image Sensors

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ABSTRACT

This paper presents a real-time calibration scheme for a 14-bit multi-segment, single slope ADC architecture using a 290MHz current DAC based on-chip ramp generator. The ramp generator enables the creation of a ramp with multiple slopes, allowing scaling of the ADC resolution according to a given system's shot noise limited curve. This flexibility allows various system tradeoffs to be made without the need for silicon redesign. For example, frame-rate, power dissipation, resolution, and other system-level parameters can be traded off to optimize performance for different applications, pixel characteristics or operating modes. Non-idealities resulting from the multi-slope ramp degrade the converter's linearity. A real-time calibration scheme was developed that greatly improved the converter's linearity and proved to be an enabling technology for the chosen ADC architecture.

I. INTRODUCTION

Given the high-speed operation of this multi-segment, single-slope ADC, there is a need for real-time calibration. Uncorrected analog temporal delays inherent to the ADC datapath can translate to significant linearity errors at the slope boundaries as shown in Figure 1. The piece-wise linear ramp transfer function can be linearized by the system, given the following conditions: 1) The segment ramp rates must be binary base 2 multiples of one another, and 2) The system must have information about where the ramp segment 'knee' was actually seen by the ADC datapath. Item 1) is addressed through careful circuit design and item 2) is addressed via the real-time calibration scheme presented in this paper.

II. COLUMN-PARALLEL ADC AND RAMP GENERATOR ARCHITECTURE

Figure 2 shows a block diagram of the column-parallel ADC architecture that is composed of the high-speed ramp generator, ADC sample network and ADC datapath. The ADC datapath is built from a low-gain preamp, high-gain comparator and two banks of SRAM. The ADC datapath employs an autozero scheme that will store the preamp and comparator voltage offsets during every row operation.

Shown on the right hand side of Figure 2 is a block diagram of the ramp generator, which is composed of 40 blocks of 64 unit current DAC cells. This yields a total step count of 2560 and each of the 40 blocks can be configured to ramp with binary-scaled ramp rates. The ramp generator is a current-mode accumulating DAC that is clocked at 290MHz. Using this scheme, the ADC can configure multiple segments with knees for a great deal of flexibility to optimize system level performance for a wide range of applications.

III. LINEARITY ERRORS AT TRANSITIONS

There is a measurable temporal delay through the ADC datapath, resulting in a time delta between when the ramp crosses the sampled input value and when the output of the ADC latches an appropriate value into the SRAM. If the ramp is moving linearly, this is indistinguishable from a voltage offset.

However, a major source of error occurs at the transition points between ramp segments, when the ramp rate changes. A change in the ramp rate at the input of the ADC will not be perceived at the ADC output until after the datapath temporal delay. This time delay must be measured and accounted for when reconstructing linear output data from the multi-sloped ADC data. Furthermore, the time delay will vary across ramp rate, temperature, supply voltage, and Monte-Carlo mismatch. This necessitates a scheme to continuously monitor these delays (used as calibration coefficients) for each knee point in each of the column-parallel ADCs.

IV. IMPLEMENTATION OF THE REAL-TIME CALIBRATION SCHEME

Figure 3 shows the scheme that was implemented to permit real-time calibration coefficient acquisition via insertion of a few extra row operations at the end of each imaging frame. The scheme configures the ramp generator for a straight ramp with no segments at a particular ramp rate (e.g. 14-bit). The actual ramp output is used to sample a programmed code value directly into the ADC sampling network. An extra conversion is then executed with a straight ramp of the previously configured bit depth. The delay value is extracted by the system as the difference between the programmed ramp sample code and the converted calibration value. The system can then apply this pure delay value to adjust the knee locations and linearize the system in the presence of significant analog delay from the ADC datapath.

As an example to further explain this real-time calibration scheme, suppose we setup the calibration mode to sample code 1200 into the ADC datapath during the calibration sampling row time. Assume that the calibration row converts a code value of 1270. This would yield a delay coefficient of 70 codes (1270-1200) for this particular ramp segment bit depth and the system would then shift the knee for this ramp segment by 70 codes.

This ADC scheme has the capability to refresh the calibration delay coefficients for every column and one ramp segment bit depth on a frame-wise basis. All ramp segments are cycled from frame to frame, though each bit depth in successive frames. Under most circumstances, it has been found that updating the delay coefficients every frame is not necessary. However as environmental or system conditions change, such as power supply voltage or temperature, updating of the coefficient matrix can improve ADC robustness and overall performance.

A configuration tool was developed to optimize the setup of the ADC for a shot noise limited response, given a pixel's conversion gain and other variables. The user can enter the desired row time, min and max resolutions and other system-level parameters. The tool will then calculate the actual voltage range that is digitized, along with outputting the knee program points for programming of the sensor's register space.

V. EXPERIMENTAL RESULTS

The imager's register space was programmed to setup a multi-segment ramp utilizing 14-13-12-11-10 bit-depth segments. Figure 4 shows the input voltage vs. output code transfer function for a single ADC column, with the real-time calibration scheme disabled and then enabled. We can see that without calibration there are noticeable kinks in the transfer function where the ramp knee points exist in the transfer function. Enabling the calibration removes these kinks from the transfer function and greatly improves the ADC performance. It should be noted that this data was acquired through a test mode, for which an external voltage is driven through column-wise source followers into the ADC sample network.

Figure 5 shows the ADC's DNL performance with the same imager setup described in the previous paragraph. A dramatic improvement is observed in the DNL performance of the ADC system when the real-time calibration scheme is enabled. Note the DNL units are in 14-bit LSB's and the 13-bit through 10-bit segments are normalized to the 14-bit LSB space. As mentioned in Section IV, this calibration data can be reacquired on frame basis and applied to the output data at the discretion of the system.

VI. CONCLUSION

A high-speed multiple segment single-slope ADC was developed with a real-time calibration scheme to enable system-level optimization and performance improvement. The ADC's real-time calibration scheme was proven to greatly improve the converter's linearity and permit flexible segment setup for a wide range of possible imaging applications.

REFERENCES

[1] Toshinori Otaka, et al., "12-Bit Column-Parallel ADC with Accelerated Ramp", IISW, 2005.

[2] Huang et. al., "Design of a PTC-Inspired Segmented ADC for High Speed Column Parallel CMOS Image Sensor", *Proc. of 2011 International Image Sensor Workshop, Hokkaido, Japan*, 2011.
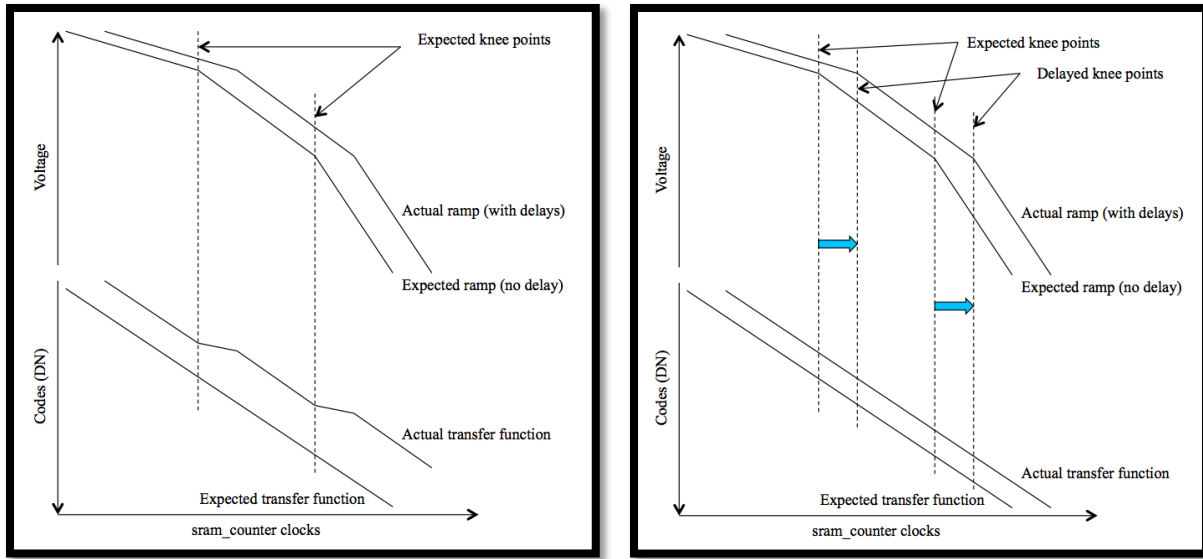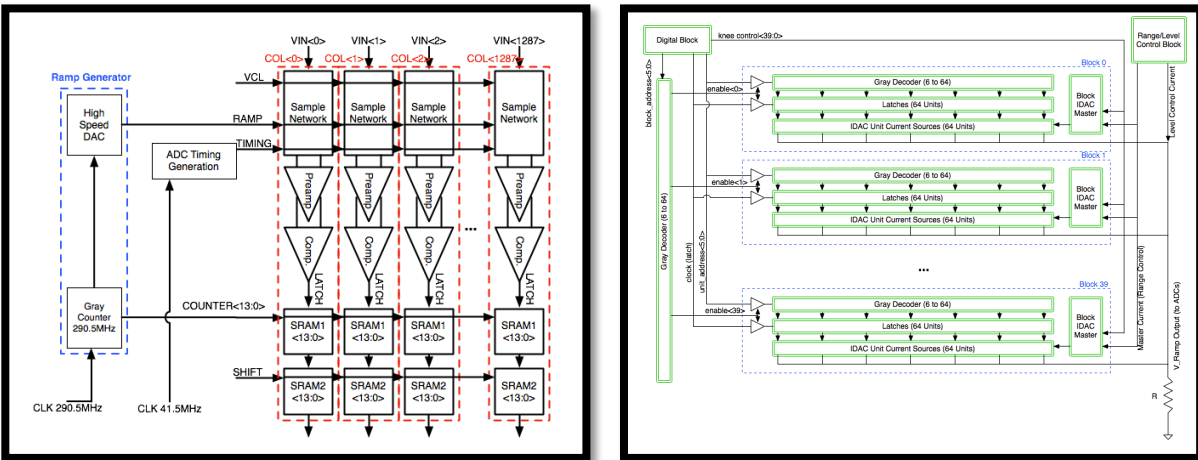
Figure 1: Need for Ramp Knee Calibration

Figure 2: Column-Parallel ADC and Ramp Generator Block Diagram
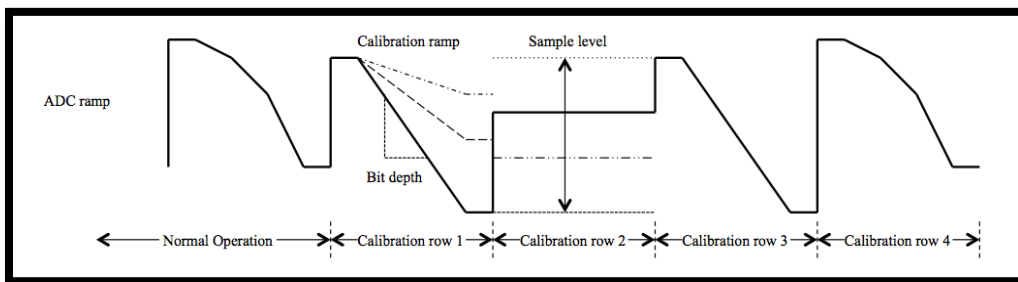

Figure 3: Real-Time Calibration Sampling and Timing Scheme
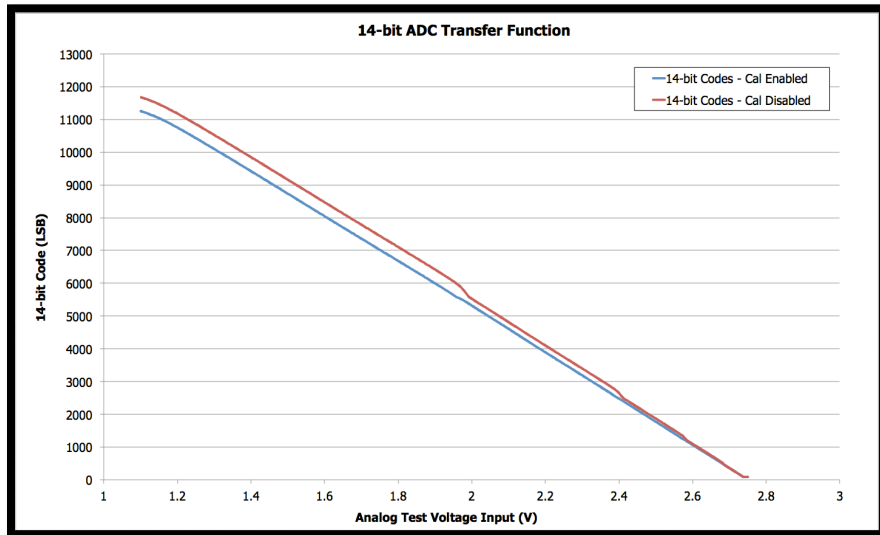
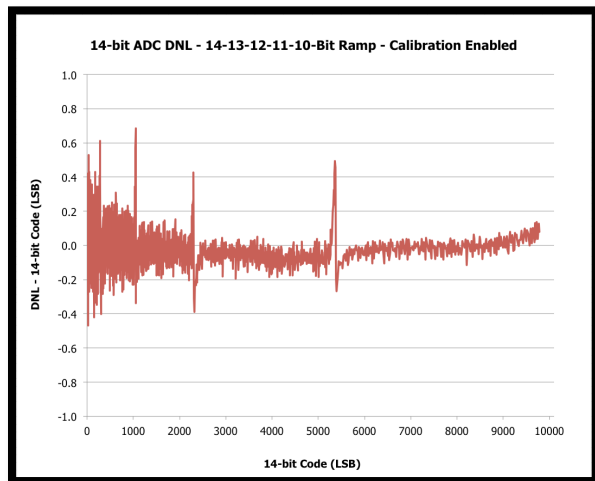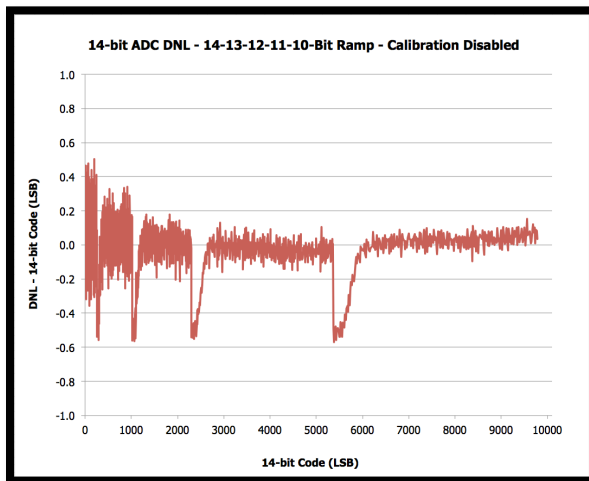Figure 4: ADC Transfer Function with and without Real-Time Calibration

Figure 5: 14-bit ADC DNL with Real-Time Calibration Disabled and Enabled