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High frame-rate global shutter image sensor with dual-reset branch SAR ADC architecture

Daniel Van Blerkom, Jeff Rysinski, Yingying Wang, Kevin Stevulak, Christophe Basset,
Loc Truong, Rami Yassine, Guang Yang, Chao Sun, Kai Ling Ong, Steve Huang

Forza Silicon Corporation, 2947 Bradley Street, Suite 130, Pasadena, CA 91107, USA
tel: +1 626 796 1182, email: dvb@forzasilicon.com

Abstract
This paper describes a high-speed 1.3Mpix global shutter CMOS image sensor with a column parallel SAR ADC readout. In order to achieve the row time requirements at the maximum frame rate, the SAR ADC utilizes a novel dual-reset branch architecture. This approach allows for overlap in the reset sampling phase, without requiring the duplication of the binary weighted capacitors and switches. The time previously used for reset sampling can be reclaimed for the ADC conversion, and the comparator power can be lowered in exchange for a relatively small area penalty. Even though the 5T global shutter pixel does not support direct CDS, the low noise analog signal chain allows us to successfully operate using external CDS for a -6dB noise improvement.

Introduction

High-speed global shutter image sensors are essential in many scientific, industrial and military applications. They also present significant design challenges, not least of which is the fast row time required. The row time consists of the row-wise pixel readout into column sample and hold capacitors, followed by ADC conversion, as shown in Figure 1. Shrinking the pixel readout time requires faster settling from the pixel outputs, which requires more power. Shrinking the ADC conversion time also requires increasing the power and area required.

One approach to relaxing the timing is to pipeline the pixel readout and ADC conversion so that each operation can use a full row time to finish, by, for example, ping-ponging between two ADCs that run at half the row-rate. This is expensive in terms of area, due to the duplication of the circuitry. In addition, differences in the comparator characteristics and the binary weighted capacitor matching can lead to offsets between the ping-ponged ADCs.

Dual-reset branch SAR ADC

We describe a different approach that promises a good balance between speed increase and the power and area impact. Instead of duplicating the entire ADC structure, only the reset-side branch is duplicated. This allows the storage of the reset level to be ping-ponged between the two reset-side branches, and for this operation to overlap with the ADC conversion of the previous pixel sample. Since the same comparator and binary weighted capacitor bank is used for all conversions, any ping-pong artifacts due to mismatches are limited to the reset side capacitor matching.

The schematic for the dual-reset branch ADC used in the sensor is shown in Figure 2. This ADC is based on the segmented ADC design described in [1]. It uses bottom plate sampling for the input signal injection, and an auto-zeroing three-stage comparator. The ADC operation proceeds initially with a coarse conversion, which determines the top 2 bits and selects the appropriate pair of references for the fine conversion, which then provides the bottom 8 bits. The 5 ADC reference voltages can be set to implement a linear 10 bit result by choosing a constant voltage difference between each pair of references, or an “accelerated-ramp” non-linear conversion which exploits the photon shot noise characteristic of light to provide finer LSB resolution at low codes (see [1,2]).

The ADC input is driven by a switched-capacitor programmable gain amplifier (PGA). The PGA is in reset while the pixel signal level is read, and the PGA reset voltage is stored in the idle ADC reset branch. When the previous ADC conversion has finished, the pixel reset level is read, producing the gained pixel voltage at the PGA output, which is sampled by the ADC signal branch. Then ADC conversion proceeds, using the reset branch just sampled, and freeing the other reset branch for sampling the PGA reset for the next conversion.

Sampling the PGA reset level for each conversion implements correlated double sampling (CDS) on the PGA output, suppressing low frequency noise and column-wise FPN due to amplifier offset variations. The ADC conversion time is designed to be 1 usec, and on-chip flexible timing generation allows for the timing to be optimized for each bit.

Layout
The column parallel ADC layout is designed for a 7.5um pitch, using Tower Semiconductor's 0.18um CIS process. The column layout includes the digital logic that selects the appropriate reference pair for the fine conversion, based on the first two coarse conversions. The binary weighted capacitors are implemented with MIM capacitors, whereas the reset branch capacitors are implemented with a higher density front-end capacitor; this further reduces the area overhead of the dual-reset branch scheme, compared with using MIM capacitors for both. Since the architecture is single-ended, capacitor matching is not critical between the signal and reset branches; the reset capacitor is sized so that it is nominally the same as the sum of the signal capacitors, in order to equalize the impedance at the inputs of the comparator and provide cancellation of common mode noise on the references. Because the PGA output needs to route through the reset branches to the signal branch, care had to be taken in the layout to ensure that the overlapping reset sampling process did not corrupt the conversion process.

Offset measurements
We measured the offset introduced due to the ping-pong of the reset branch to be less than 2mV. This offset is removed in our application with black frame subtraction. We believe the offset is due to the mismatch in the routing of the two reset branches, due to the placement of the reset capacitors in the column.

External CDS
Our image sensor uses a 5T global shutter pixel. Compared to a 7T pixel, the 5T pixel has a better shutter rejection ratio and does not require a TX transfer to read out, making it more amenable to high-speed operation. However, it does not allow for direct CDS, in that the pixel's reset level is not available at the same time as its signal level, leading to a relatively high sensor noise floor of 28 e-.
By capturing a frame of reset levels prior to integration, followed by a frame of signal levels after integration, CDS can be accomplished externally. The low noise analog readout allows us to reduce the noise floor to 12.6 e- using external CDS, as seen in Figure 3.
Of course, the drawback of external CDS is that the effective frame rate is reduced by a factor of 2. In addition, the digital subtraction of the reset levels, which in our sensor varied by about +/- 50mV within a frame, affects the uniformity in saturation and limits the maximum output code.

Summary
We designed, fabricated and tested a column parallel 3000 fps 1.3Mpix global shutter sensor utilizing a novel dual-reset branch SAR ADC. This SAR architecture allows for the overlap of the sampling of the reset level of the next pixel with the conversion of the current pixel. We confirmed operation of the ADC and measured the offset introduced, which is removed in our application with black frame subtraction. We also measured a -6dB reduction in the sensor noise floor when using external CDS.

References:
[1] Huang et al., **"Design of a PTC-Inspired Segmented ADC for High Speed Column Parallel CMOS Image Sensor"**, *Proc. of 2011 International Image Sensor Workshop*, Hokkaido, Japan, 2011.
[2] Otaka et al., **"12-Bit Column-Parallel ADC with Accelerated Ramp"**, *Proc. of 2005 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Karuizawa, Japan, 2005.

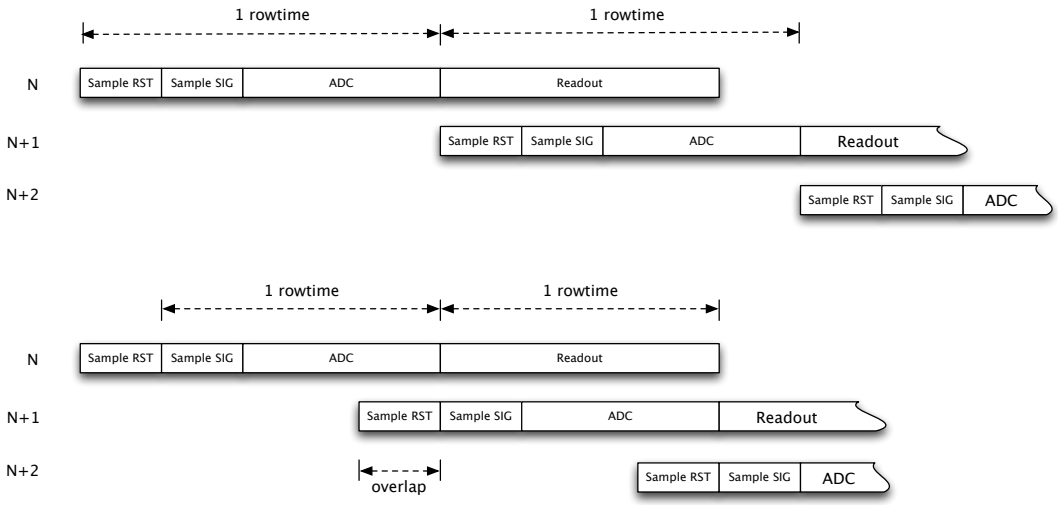

Figure 1 – Timing without (top) and with (bottom) dual reset branch sampling

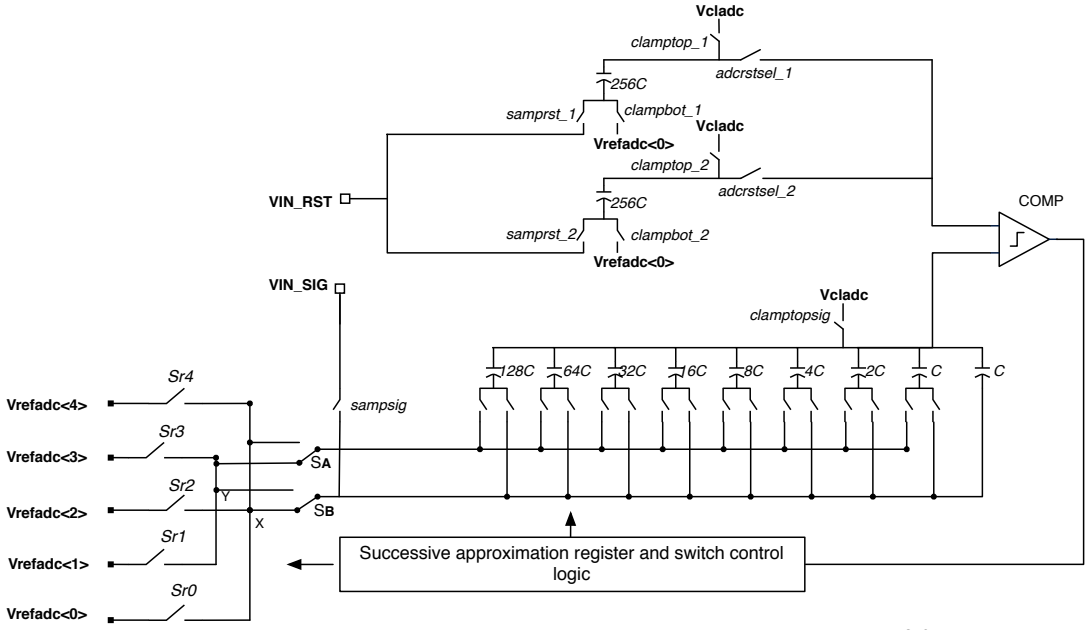

Figure 2 – Dual Reset Branch SAR ADC

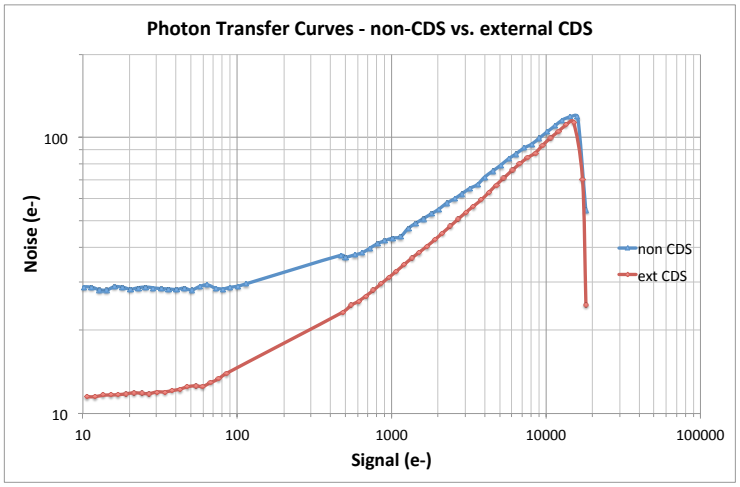

Figure 3 – PTC Curve for non-CDS and external CDS operation

Number of pixels	1296 x 1040
Pixel pitch	15 um
Pixel type	5T global shutter
Frame rate	3000 fps
Read noise	28 e- rms (non-CDS) 12.6 e- rms (ext-CDS)
Shutter	global shutter
Shutter rejection	>20000:1
ADC	2+8 bit SAR ADCs
Output interface	LVDS 350MHz DDR
Power consumption	approx. 4 W
Process	0.18um CIS process

Table 1 – Sensor Specifications

Figure 4 – Captured image from the sensor at 1000 fps, 80 msec after impact.