2.1 A 4-Side Tileable Back Illuminated 3D-Integrated Mpixel CMOS Image Sensor

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The dominant trend with conventional image sensors is toward scaled-down pixel sizes to increase spatial resolution and decrease chip size and cost [1]. While highly capable chips, these monolithic image sensors devote substantial perimeter area to signal acquisition and control circuitry and trade off pixel complexity for fill factor. For applications such as wide-area persistent surveillance, reconnaissance, and astronomical sky surveys it is desirable to have simultaneous near-real-time imagery with fast, wide field-of-view coverage. Since the fabrication of a complex large-format sensor on a single piece of silicon is cost and yield-prohibitive and is limited to the wafer size, for these applications many smaller-sized image sensors are tiled together to realize very large arrays [2,3]. Ideally the tiled image sensor has no missing pixels and the pixel pitch is continuous across the seam to minimize loss of information content. CCD-based imagers have been favored for these large mosaic arrays because of their low noise and high sensitivity, but CMOS-based image sensors bring architectural benefits, including electronic shutters, enhanced radiation tolerance, and higher data-rate digital outputs that are more easily scalable to larger arrays. In [4] we report the first back-illuminated, 1Mpixel, 3D-integrated CMOS image sensor with 8μm-pitch 3D via connections. The chip employs a conventional pixel layout and requires 500μm of perimeter silicon to house the support circuitry and protect the array from saw damage. In this paper we present a back-illuminated 1Mpixel CMOS image sensor tile that includes a 64-channel vertically integrated ADC chip stack, and requires only a few pixels of silicon perimeter to the pixel array. The tile and system connector design support 4-side abuttability and fast burst data rates.

Figure 2.1.1 shows a schematic of the digital imaging tile's 7-layer (or tier) physical structure. The first 2 tiers are a 3D imager, and the supporting 5 tiers are a multichip silicon stack. 3D integration is exploited in 2 different methods, each at different pitch scales. The 3D imager is a 2-tier 1024×1024 pixel image sensor array fabricated with 8μm-pitch, per-pixel 3D vias. The imager is vertically connected to the silicon stack through a gold stud bump array at 500μm pitch. Tier 1 consists of 100% fill factor, deep-depletion photodiodes, thinned to 50μm. Tier 2 consists of SOI-CMOS pixel readout and selection circuitry that is 3D-connected to Tier-1 photodiodes. Pixels extend to the edge of the 3D imager. A 5-layer silicon cube provides a digital system interface and also serves as a mechanical support to the thinned imager. Cube stack bus lines pass on two faces and an array of pogo pins provide a re-attachable flexprint/system interface connection. Both the silicon stack and system interface connectors fit within the shadow of the 3D imager, allowing close placement of neighboring tiles.

Figure 2.1.2 describes the tile block diagram and pixel circuit. Tiers 1 and 2 comprise the pixel array. The silicon stack includes 2 silicon chips with 64, 12b pipelined ADCs, a timing sequencer, an image tile address encoder, bias generators, an Inter-Integrated Circuit (I^2C) serial interface, and two 12b wide LVDS outputs operating at 512Mb/s/channel. Imager control is programmable to select readout mode (e.g. snapshot, rolling read, frame sub-sampling) and ADC timing and settings. The pixel consists of a photodiode, a reset transistor (RST), a snapshot transistor (S), a row select switch (RS), and a source follower. The analog signal from the 1024 columns is multiplexed onto 64 outputs that are fed through bump bonds to the ADCs in the silicon chip stack.

Only a few pixels of perimeter silicon surrounds the edge of the pixel array, since the CMOS support circuitry, traditionally located outside the pixel array, is now embedded within it. The Tier-2 pixel circuitry ($8.0\times8.0\mu m^2$) is undersized relative to the Tier-1 photodiode footprint ($8.3\times8.3\mu m^2$) and Tier-1 metallization is used as a vertical fanout. Figure 2.1.3 shows how the extra space is aggregated in blocks of 16×16 to create "streets" and "avenues" that are used for distribution of selection transistors, amplifiers, and ESD protection. In addition, a deep-trench process [5] is implemented to avoid physical damage to edge pixels and provide a continuous backside connection to the photodiode to permit deep-depletion operation for a broad spectral response.

A cross-sectional SEM micrograph through several 8μm pixels of a functional active pixel imager is shown in Fig. 2.1.4. A 3D via connects Tier-2 fully depleted SOI CMOS metal-3 to Tier-1 (diode) metal-3, and a back-metal cap (BM-1) covers the 3D via plug. The uppermost level of back metal (BM-2) is thicker and is used for a bump-bonding interface. The 50nm-thick SOI transistor features can be seen near the top of the SEM. Pixel-to-pixel photodiode isolation is accomplished through implantation alone, thus realizing much lower dark currents than STI-isolated pixels.

Figure 2.1.5 is a raw 1Mpixel image taken by the CMOS image sensor tile. The tile is temporarily mounted to a quartz wafer and the release holes provide ports for solvent removal of the quartz. The fixed-pattern noise is systematic and is related to the metal fanout and layout compression methods used to minimize seam loss. Imaging performance is observed to edge of the pixel array. Figure 2.1.6 summarizes characteristics for the back-illuminated sensor described in this paper. The chip's overall performance is tested in an FPGA-based system. The board supports a 4-tile row and is stackable to support additional tile rows. It includes LVDS receivers, SRAM data storage, and a camera link interface to a remote computer. No on-chip noise reduction methods are employed; we are working to understand the noise performance. Other design revisions could improve the sensitivity and stack power dissipation. The principal pixel yield detractor arises from column or row dropouts; greater redundancy in architecture and layout would minimize vulnerability to single-point defects.

Figure 2.1.7 is a photograph of the completed sensor tile showing the locations of the various circuit blocks. This is the first report of a 4-side-abuttable, vertically integrated, "photons-to-bits" image sensor tile; it achieves only a few pixels-equivalent of seam loss. This work demonstrates a path toward high-data-rate 3D image sensors and the methods developed here are extendable to other architectures, such as CCDs, APDs, or infrared focal-plane arrays.

Ackowledgments:
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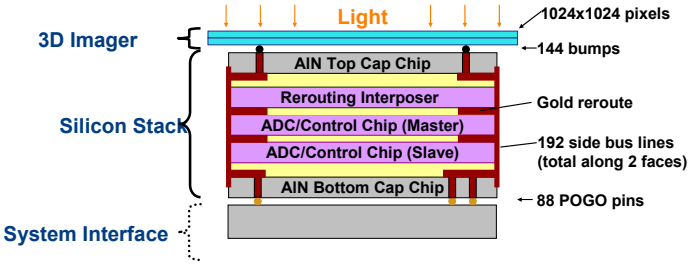

Figure 2.1.1 Schematic diagram of the 4-side-abuttable, 3D-integrated, CMOS imaging tile.

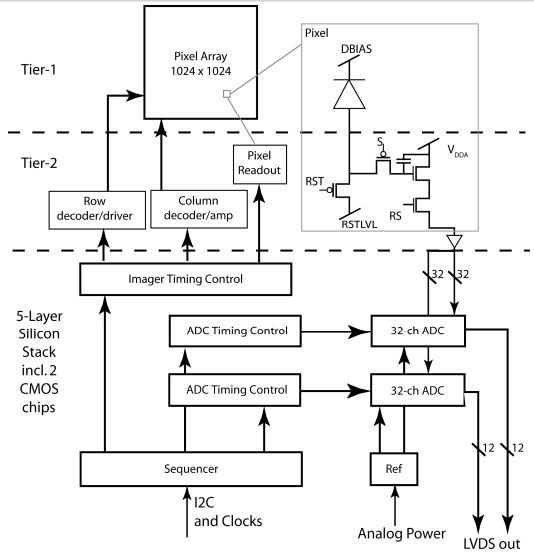

Figure 2.1.2 Tile block diagram and pixel circuit.

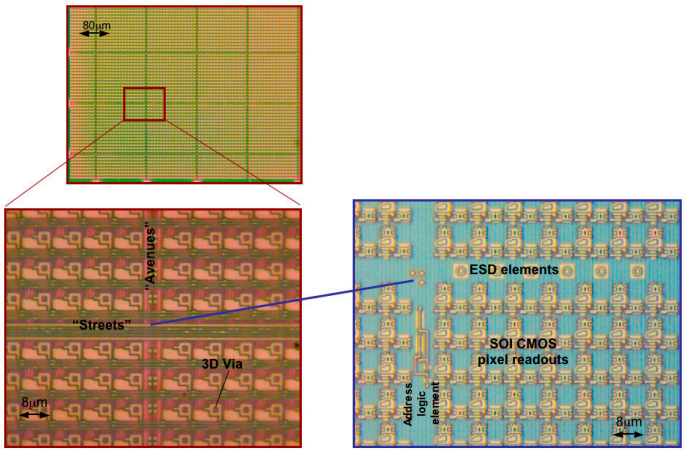

Figure 2.1.3 Die micrograph details of Tier-2 pixel readouts. CMOS addressing logic is embedded into space aggregated in streets and avenues. The rightmost image shows polysilicon and SOI active layers captured before formation of metal layers.

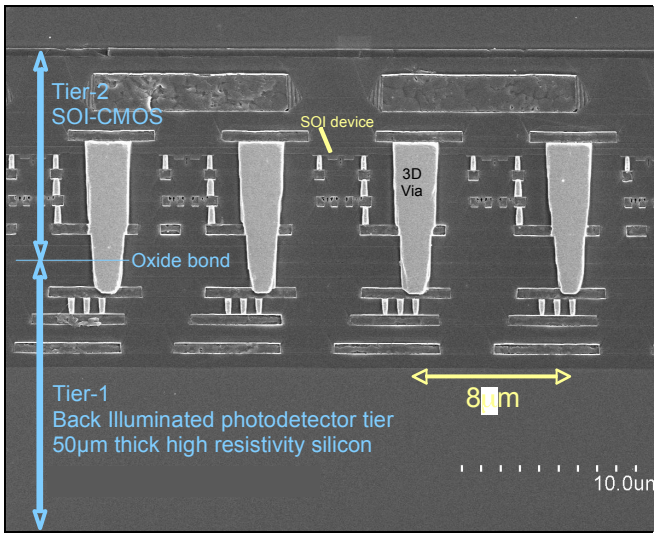

Figure 2.1.4 Cross-sectional SEM micrograph through functional 3D-integrated active pixel imager.

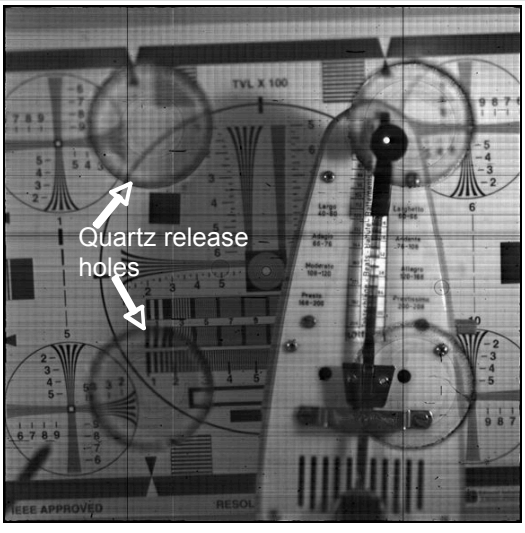

Figure 2.1.5 Captured raw image from digital tile at 10fps, with digital data read out in 1ms.

Parameter	Value	Comment
Process Technology	Tier 1: p+n diode in 3000Ω-cm, FZ-Si Tier 2: 0.35µm MIT-LL SOI CMOS 3.3V Stack: 0.35µm Tower 2P4M 3.3V	
Pixel Array size	8.5 mm (H) x 8.5 mm (V)	
Chip stack size	8.0 mm (H) x 8.0 mm (V)	
Pixel Array format	1024 x 1024	
Diode pixel size	8.3µm (H) x 8.3µm (V)	
Readout pixel size	8.0µm (H) x 8.0µm (V)	Address circuitry embedded in "streets" and "avenues"
Pixel Fill Factor	100%	Back illuminated
Tile Fill Factor	99.7%	Few pixel border surrounding pixel array
Tile-to-Tile seam loss	few pixels	plus mechanical placement error
Pixel type	4-T, Snapshot	Rolling read and sub-sampling also supported
Pixel Operability	>99.6%	
Signal chain capacity	2V (130ke-)	
Responsivity	16 µV/e- (est.)	Estimated from sense node capacitance
Diode Dark current at RT	< 200 fA/pixel	
Temporal noise	5.5mVrms (350e- rms)	
Analog/Digital Conversion	32 channels per chip 12-bit pipelined ADC	2-ADC chip set in Irvine Stack
Conversion time	1.024 msec	
Digital interface	Two 12-bit-wide outputs	
Digital data rate	512 Mbit/sec LVDS	
Tested frame rate	10 fps	1% duty cycle for ADC
3D Imager Power	0.23 mW/Mpix/sec	At 10fps
ADC/Control Power	6.65mW/Mpix/sec	At 10fps

Figure 2.1.6 Performance summary.

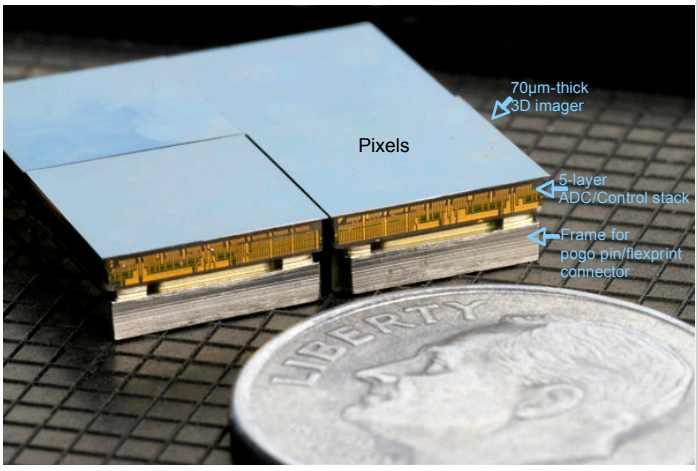

Figure 2.1.7: Photo of 4-side-abuttable, 3D-integrated, digital imaging tile.

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